UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,369	08/06/2003	Richard W. Adkisson	200208998-1	1303

23413 7590 01/14/2008

CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2117	

MAIL DATE	DELIVERY MODE
01/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/635,369	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08062003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are currently pending in the application. Claims 12-17 are withdrawn from consideration due to the Election/Restriction requirement below. Therefore, claims 1-11 and 18-20 have been examined.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11 and 18-20, drawn to an increment/decrement circuit for use with a general purpose performance counter, classified in class 714, subclass 706.

II. Claims 12-17, drawn to a system for determining latency, classified in class 714, subclass 700.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions **I.** and **II.** are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination Group I. has separate utility such as a system for determining latency. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found

allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Attorney Steve Webb on 12/17/2007 a provisional election was made without traverse to prosecute the invention of **Group I., claims 1-11 and 18-20**. Affirmation of this election must be made by applicant in replying to this Office action. **Claims 12-17** are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

7. In order to expedite the prosecution for the subject application, **the non-elected claims should be canceled in response to this office action.**

Information Disclosure Statement

8. The information disclosure statement (IDS) submitted on 08/06/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

9. The disclosure is objected to because of the following informalities:

a.) Pages 1-2, ¶s 2-3, p. 7, ¶ 24 and p. 8, ¶ 26: The blank lines should be filled with the proper information.

b.) Page 17, ¶ 46 in relation to Fig. 6D does not appear to be correct. The accumulator circuit of Fig. 5 is 510 not 516. Fig. 6D discloses "another" embodiment of the accumulator circuit 510 of Fig. 5, not "the" embodiment. See ¶ 42 last sentence of p. 14 to first sentence of p. 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 1 recites the limitation "aligned debug data" in lines 9 and 13. There is insufficient antecedent basis for this limitation in the claim. It is the block that is aligned not the debug data. This should read "said block of debug data". Appropriate correction is required.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 4, 5, 10, 11 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by **Elliott et al.** (US-6826247), hereinafter Elliott.

Claims 1, 4, 5, 10, 11 and 18-20:

Elliott teaches an increment/decrement circuit for use with a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the increment/decrement circuit comprising: a delay circuit block (**Fig. 5, delay chain 502, the phase detectors 505**) operable to receive and align at least a block of said debug data. **Elliott** also teaches a first mask circuit connected to said delay circuit block, wherein said first mask circuit is operable to select a first portion of said block of aligned debug data for incrementing and a second mask circuit connected to said delay circuit

block, wherein said second mask circuit is operable to select a second portion of said block of aligned debug data for decrementing (**Fig. 5, the claimed first and second mask circuits are embodied in a Delay Measurement and Ambiguity Resolver (DM&AR) 512 that receives results from the delay chain phase detectors 505 and generates an increment or decrement signal to the Averaging Counter 514**). **Elliott** furhter teaches an accumulation circuit (**Fig. 5, Averaging Counter 514**) connected to said first mask circuit and said second mask circuit, said accumulation circuit for generating an accumulated value based on outputs provided by said first and second mask circuits. (Col. 8, l. 36 to col. 10, l. 28).

Claim 4:

Elliott teaches said delay circuit block (**Fig. 5, delay chain 502, the phase detectors 505**) is operable responsive to a delay_values signal (**Fig. 5, delay configuration signal**) that provides clock delaying values for each bit in said block of said debug data. (Col. 8, l. 36 to col. 10, l. 28).

Claim 5:

Elliott teaches said delay circuit block includes (**Fig. 5, delay chain 502, the phase detectors 505**) a series of registers operable (**phase detectors registers 508 and 510**) to be tapped for providing a plurality of inputs to a Multiplexer (MUX) block (**Fig. 2, non-glitching MUX 206**) that is controlled by a delay_values signal. (Col. 8, l. 36 to col. 10, l. 28).

Claims 10 and 19:

Elliott teaches said accumulation circuit (**Fig. 5, Averaging Counter 514**) is operable to forward a signal (**SUM**) indicative of an instantaneous outstanding transaction count based on outputs provided by said first and second mask circuits (**After the "lag" point, the Averaging Counter 514 continues to sum up the DM&AR 512 output phase measurements until the Lag/Latency Counter 516 reaches the "latency" set point, at that point the State Update Logic block 520 looks at the output sum of the Averaging Counter 514 and sends an update pulse to the Delay State Counter 518**). (Col. 10, ll. 17-60).

Claims 11 and 20:

Elliott teaches said instantaneous outstanding transaction count is forwarded to a counter circuit for further processing (**Fig. 5, Delay State Counter 518**). (Col. 10, ll. 17-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Elliott et al.** (US-6826247), hereinafter Elliott.

Claims 2 and 3:

The limitations of claims 2 and 3 (said block of said debug data comprises 16 bits (claim 2) and said block of said debug data forms a portion of an 80-bit wide debug data signal, (claim 3)) constitute and obvious design choice and would be have been obvious to one of ordinary skill in the art at the time the invention was made. The artisan would be motivated to do so because a person of ordinary skill in the art has good reason to pursue the known options of various bus sizes within his or her technical grasp.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Elliott et al.** (US-6826247), hereinafter Elliott in view of **Joo** (US-5913229), hereinafter **Joo**.

Claim 6:

Elliott does not explicitly teach said first mask circuit comprises an AND block having a plurality of 2-input AND gates for bit-wise ANDing said block of said debug data with a multi-bit inc_mask signal. However, **Elliott** does teach the Delay Measurement and Ambiguity Resolver (DM&AR) 512 that receives results from the delay chain phase detectors 505 and generates an increment or decrement signal to the Averaging Counter 514. **Joo** teaches in an analogous art a masking circuit 330 that is constructed with an **AND gate 318** which receives the data of the barrel shifter 317 and 16 bit mask data for the number of bits of the sample data. (Fig. 3, col. 3, l. 36 to col. 4, l. 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize **Joo's** masking circuit 330 in **Elliott's** DM&AR 512. The artisan would be motivated to do so because a person of ordinary skill in the art has

good reason to pursue the known options of masking two signals with an AND circuit as claimed within his or her technical grasp.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Elliott et al.** (US-6826247), hereinafter Elliott in view of **Mann** (US-6275782), hereinafter Mann.

Claim 7:

Elliott does not explicitly teach *said first mask circuit comprises: an XOR block having a plurality of XOR gates for bit-wise XORing said block of said debug data with a multi-bit inc_invert signal to generate a multi-bit output signal; and an AND block having a plurality of 2-input AND gates for bit-wise ANDing said multi-bit output signal with a multi-bit inc_mask signal.* However, **Elliott** does teach the Delay Measurement and Ambiguity Resolver (DM&AR) 512 that receives results from the delay chain phase detectors 505 and generates an increment or decrement signal to the Averaging Counter 514. **Mann** teaches in an analogous art ANDing together clock signal 209 (*multi-bit inc_mask signal*) and the output from XOR gate 207 (*multi-bit output signal*) to provide a gated clock signal 210 to the counter. (Fig. 2, col. 3, ll. 20-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize **Mann's** AND-XOR circuit in **Elliott's** DM&AR 512. The artisan would be motivated to do so because a person of ordinary skill in the art has good reason to pursue the known options of masking two signals with an AND-XOR circuit as claimed within his or her technical grasp.

15. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Elliott et al.** (US-6826247), hereinafter Elliott in view of **Neukom** (US-20010005408), hereinafter Neukom.

Claim 8:

Elliott does not explicitly teach *said accumulation circuit comprises a first population count circuit coupled to said first mask circuit a second population count circuit coupled to said second mask circuit and an adder circuit coupled to said first population count circuit and said second population count circuit.* However, **Elliott** does teach the Averaging Counter 514 continues to sum up the DM&AR 512 output phase measurements until the Lag/Latency Counter 516 reaches the "latency" set point, at that point the State Update Logic block 520 looks at the output sum of the Averaging Counter 514 and sends an update pulse to the Delay State Counter 518. (Col. 10, ll. 17-60). **Neukom** teaches in an analogous art the accumulator adder circuit of Fig. 3 contains an increment register 30 (*first mask circuit*), a decrement register 31 (*second mask circuit*), a multiplexer 32, and adder 34 (*adder circuit*) and an accumulator register 36. The increment and decrement registers 30, 31 are coupled to a first input of the adder 34 via multiplexer. An overflow output of the accumulator 36 is coupled to the multiplexer to select which of the contents of increment or decrement register 30, 31 is fed to the first input of the adder 34. The output of the adder 34 is coupled to the accumulator 36. (Page 3, ¶ [0033]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify **Elliott's** Averaging Counter 514 to incorporate

Neukom's accumulator adder circuit. The artisan would be motivated to do so because a person of ordinary skill in the art has good reason to pursue the known options of using well known accumulator circuits within his or her technical grasp.

Claim 9:

Elliott in view of **Neukom**, as per claim 8, teaches accumulation circuit comprises a first population count circuit coupled to said first mask circuit a second population count circuit coupled to said second mask circuit. However, instead of the claimed subtract circuit, **Elliott** in view of **Neukom** teaches *an adder circuit* coupled to said first population count circuit and said second population count circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the accumulation circuit of **Elliott** in view of **Neukom** to use a subtract circuit instead of the adder circuit. The artisan would be motivated to do so because a person of ordinary skill in the art has good reason to pursue the known options of using well known accumulator circuits within his or her technical grasp as well as being an obvious design choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner
AU 2117 1/8/08

John J. Tabone, Jr. 1/8/08
Examiner
Art Unit 2117